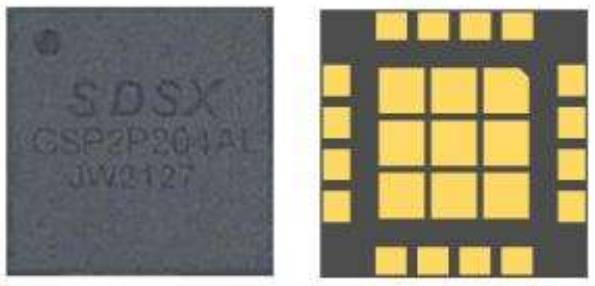
GSP2P204AL

2.1-2.2 GHz 4 W Power Amplifier



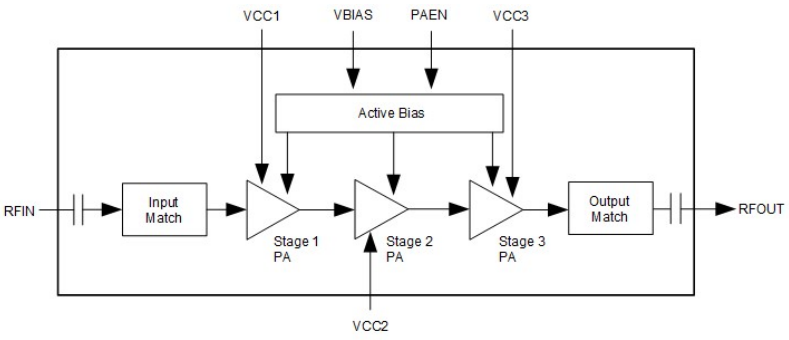
Description

The GSP2P204AL is a high-gain power amplifier (PA) with high power added efficiency (PAE) and linearity. The product is fully input and output matched to 50 Ω system. The compact 5X5 mm PA is designed for FDD and TDD 2G/3G/4G LTE small cell base stations operating from 2.1 to 2.2 GHz. The active biasing circuitry is integrated to compensate PA.

Features

- High efficiency: PAE = 34% @ +28 dBm
- High linearity: +28 dBm with < -50 dBc linearized ACLR (20 MHz LTE, 8.5 dB PAR signal)
- High gain: 39 dB
- Great input and output return loss
- Integrated enable On/Off function: PAEN = 2 V
- On chip ESD protection
- Compact package: 16-pin, 5 x 5 x 0.85 mm

Functional Block Diagram



Applications

- FDD and TDD 2G/3G/4G LTE systems
- 3GPP Band 66 along with Band 1 Small Cells
- Driver amplifier for micro-base and macro-base stations

Ordering Information

- GSP2P204AL
- GSP2P204AL-EVB

Recommended Operating Conditions

Parameter	Units	Min	Typ	Max
Supply voltage (VCC1, VCC2, VCC3, VBIAS)	V	4.75	5	5.25
PA enable (PAEN): **ON** **OFF**	 V V	 1.7 0	 2.0 0	 2.5 0.5
PA enable current	μA		1	
Operating frequency	MHz	2100		2200
Operating temperature	℃	-40	+25	+85
RF turn-on/turn-off time	μs		1	

Absolute Maximum Ratings

Parameter		Units	Min	Max
RF input power (CW, 50 Ω load, T=25℃)		dBm		+10
Supply voltage (VCC1, VCC2, VCC3, VBIAS)		V		5.5
PA enable		V		3
Operating temperature		℃	-40	+100
Storage temperature		℃	-55	+125
Junction temperature		℃		+150
Power dissipation @ +28 dBm output power		W		TBD
Device thermal resistance @ +28 dBm output power		℃/W		TBD
ESD Rating	**HBM**	V		1000
	CDM	V		TBD

Electrical Specifications

Test Conditions: 50 Ω system, VCC1 = VCC2 = VCC3 = VBIAS = 5 V, PAEN = 2.0 V, f = 2140 MHz, TC = +25 ℃;

Parameter	Conditions(1)	Units	Min	Typ	Max
Frequency		MHz	2100		2200
Small signal gain	PIN = -30 dBm	dB		39	
Gain @ +28 dBm	POUT = +28 dBm	dB		40	
Input return loss	PIN = -30 dBm	dB		-13	
Output return loss	PIN = -30 dBm	dB		-11	
Output P3dB	100 μs/1 ms, 10% duty cycle	dBm		36	
Saturated Output Power	100 μs/1 ms, 10% duty cycle	dBm		36.3	
Power Added efficiency(2)	POUT = +28 dBm	%	31	34	
ACPR(Uncorrected)(2)	POUT = +28 dBm	dBc		-28.5	
ACPR(Uncorrected)(3)	POUT = +28 dBm	dBc		-26.5	
ACPR(Corrected)(2)	POUT = +28 dBm	dBc		-51	
Quiescent current	No RF signal	mA		120	
Total Operating Current	POUT = +28 dBm	mA		380	
Thermal Resistance		℃/W		TBD	
2nd harmonic	CW, POUT = +28 dBm	dBc		-34.3	
3rd harmonic	CW, POUT = +28 dBm	dBc		-39.3	

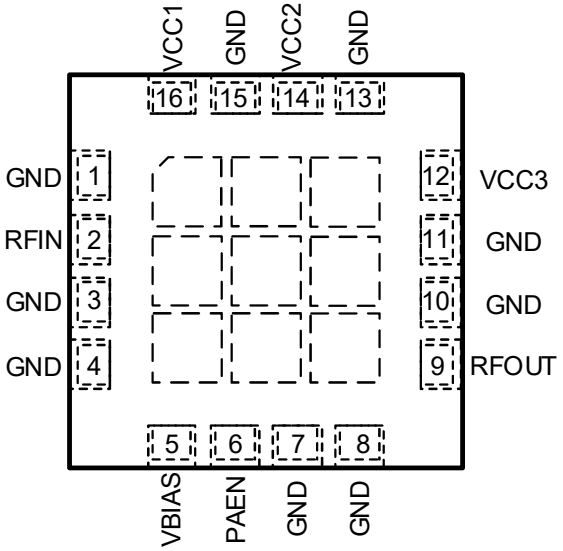
Notes:

1. Test conditions unless otherwise noted: All VCC & VBIAS = +5.0 V, PAEN = +2 V, Temp = +25 ℃, 50 Ω system, f = 2140MHz

2. LTE, 20 MHz E-UTRA Test Model 1.1 or 3.1, PAR = 8.5 dB

3. LTE, 20 MHz x 3 E-UTRA Test Model 1.1 or 3.1, PAR = 8.5 dB

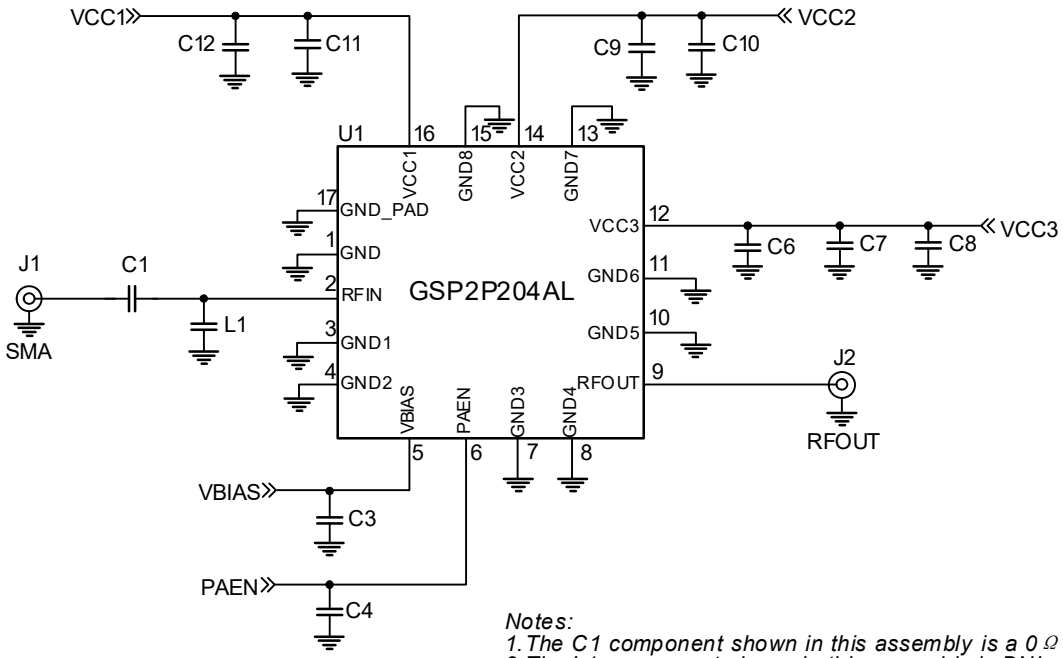
Pin Assignments and Description



Pin	Name	Description
1	**GND**	Ground
2	**RFIN**	RF input port
3	**GND**	Ground
4	**GND**	Ground
5	**VBIAS**	Bias voltage
6	**PAEN**	PA enable
7	**GND**	Ground
8	**GND**	Ground

Pin	Name	Description
9	**RFOUT**	RF output port
10	**GND**	Ground
11	**GND**	Ground
12	**VCC3**	Stage 3 collector voltage
13	**GND**	Ground
14	**VCC2**	Stage 2 collector voltage
15	**GND**	Ground
16	**VCC1**	Stage 1 collector voltage

PCB Evaluation Board Schematic



Notes:
1. The C1 component shown in this assembly is a 0 Ω resistor.
2. The L1 component shown in this assembly is DNI.

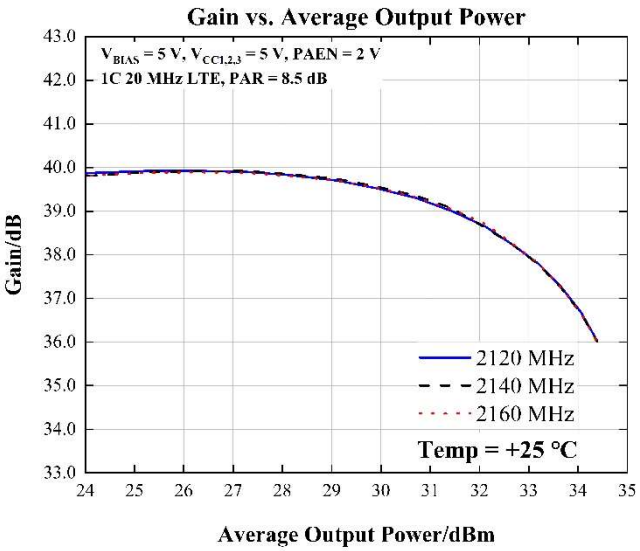
Evaluation Board BOM

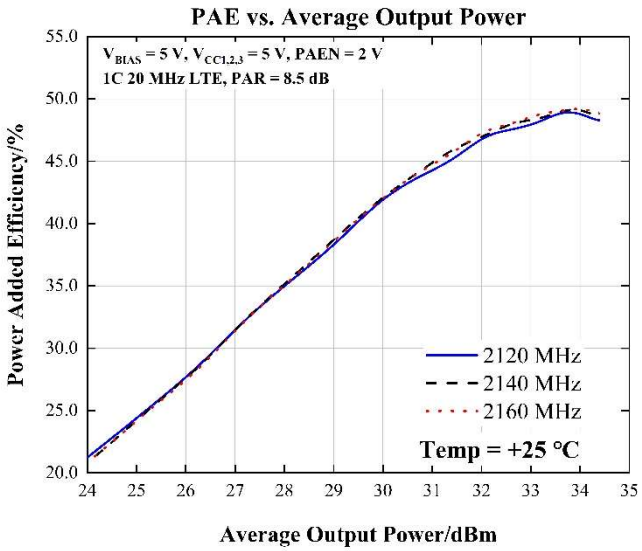
Reference Des.	Value	Manuf.	Part Num.
PCB	N/A	SDSX	GSP2P204AL-EVB
Q1	N/A	SDSX	GSP2P204AL
C1(1)	0 Ω	Murata	0402
C3, C6	1 μF	Murata	0402
C4, C7	3300 pF	Murata	0402
C9	470 nF	Murata	0402
C11	100 nF	Murata	0402
C8, C10, C12	10 μF	Murata	1206
L1	DNI		

Notes:

1.The C1 component shown in this assembly is a 0 Ω resistor.

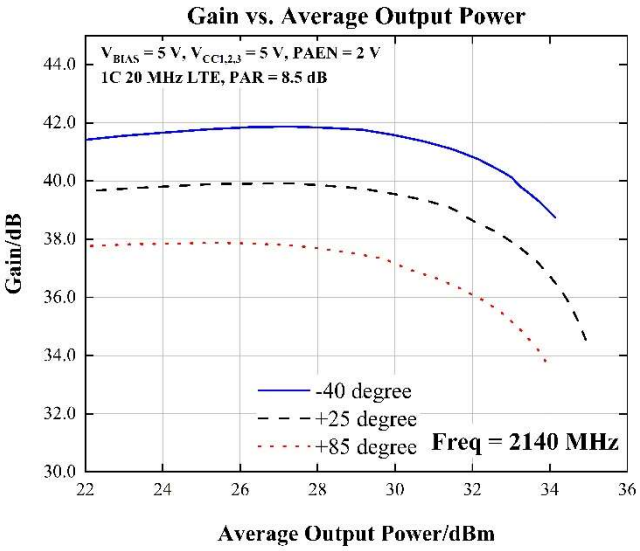
Performance Plots — LTE，Over Frequency

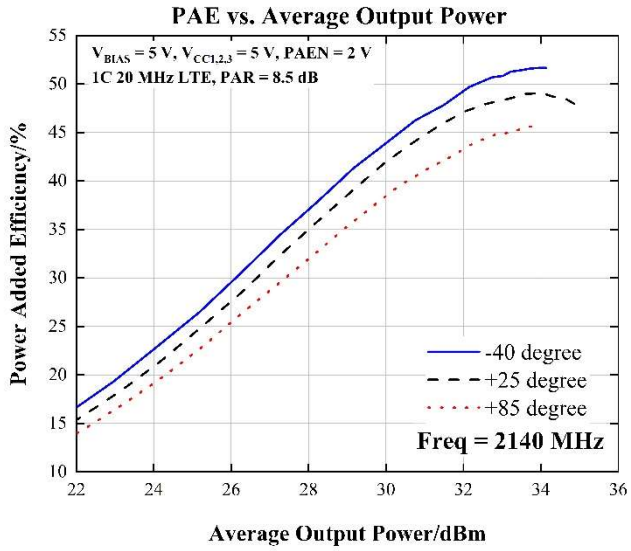




Test conditions unless otherwise noted: VBIAS = 5 V, VCC1,2,3 = 5 V, PAEN = 2 V, T = +25 °C, tested using a single-carrier, 20 MHz LTE signal with 8.5 dB PAR on a reference design fixture.

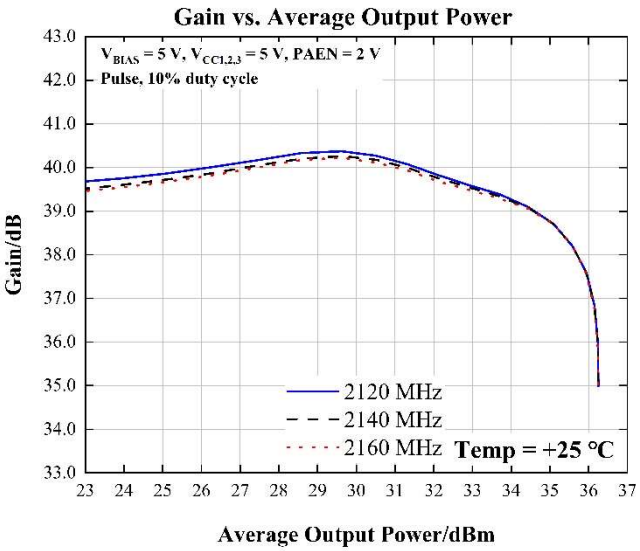
Performance Plots — LTE，Over Temperature

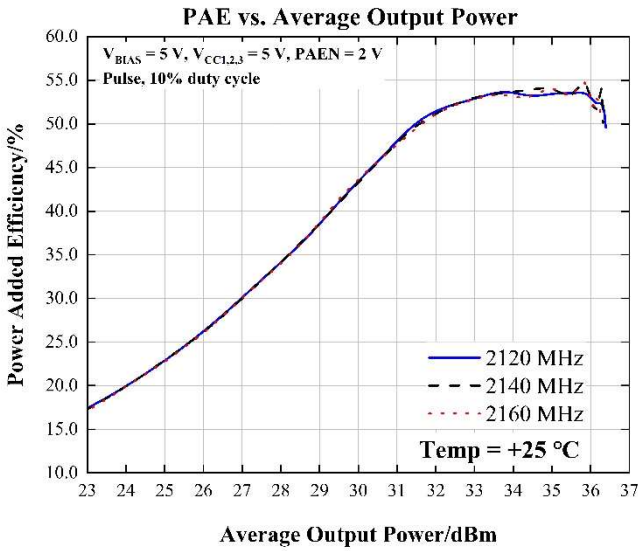




Test conditions unless otherwise noted: VBIAS = 5 V, VCC1,2,3 = 5 V, PAEN = 2 V, tested at 2140 MHz using a single-carrier, 20 MHz LTE signal with 8.5 dB PAR on a reference design fixture.

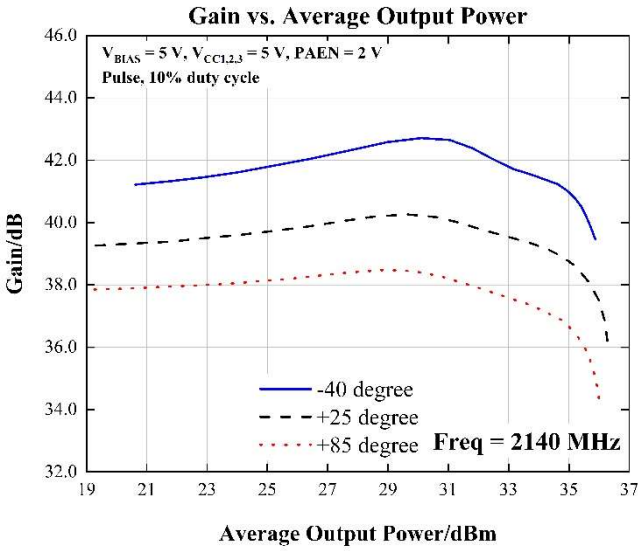
Performance Plots — Pulse Signal Measurements，Over Frequency

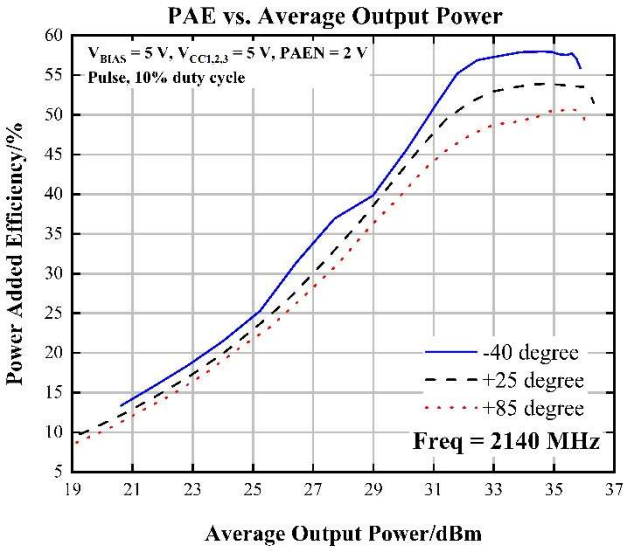




Test conditions unless otherwise noted: VBIAS = 5 V, VCC1,2,3 = 5 V, PAEN = 2 V, T = +25 ℃, tested using a pulse signal, 10% duty cycle.

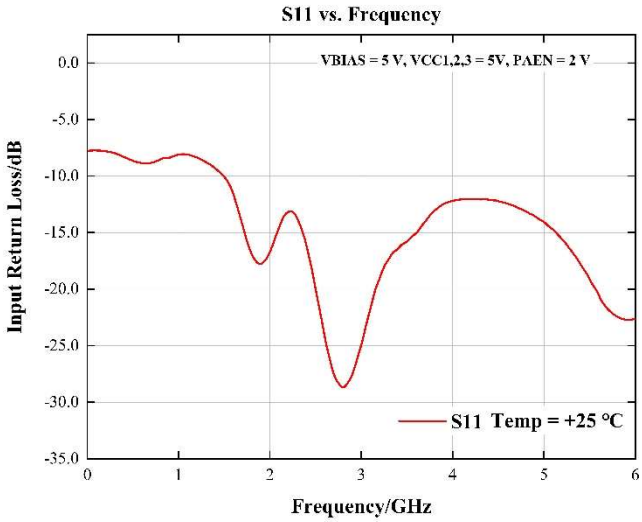
Performance Plots — Pulse Signal Measurements，Over Temperature

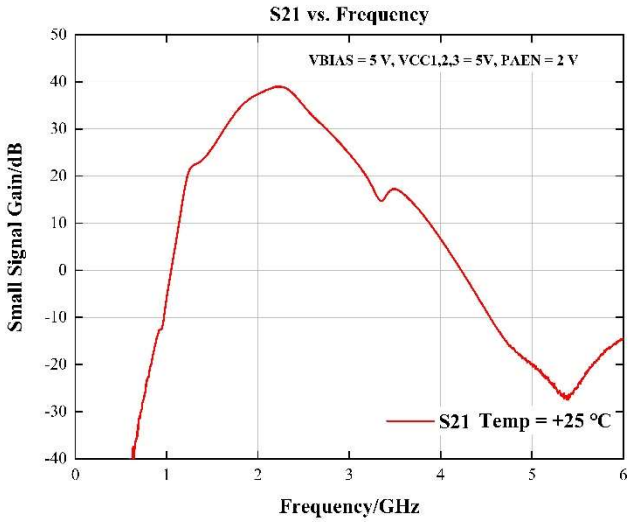


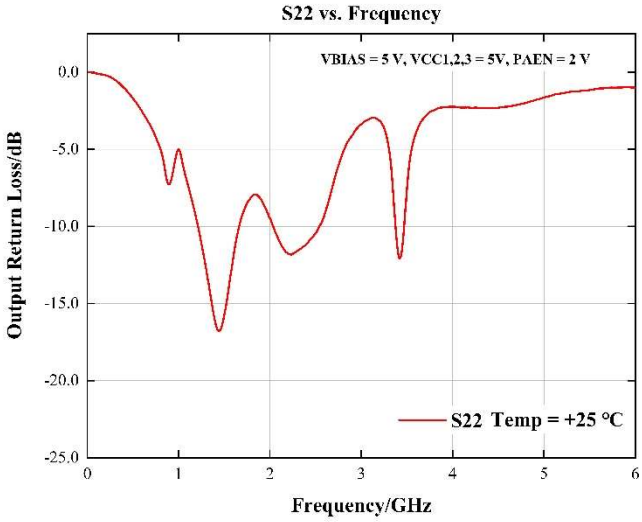


Test conditions unless otherwise noted: VBIAS = 5 V, VCC1,2,3 = 5 V, PAEN = 2 V, tested at 2140 MHz using a pulse signal, 10% duty cycle.

Performance Plots —S-parameter

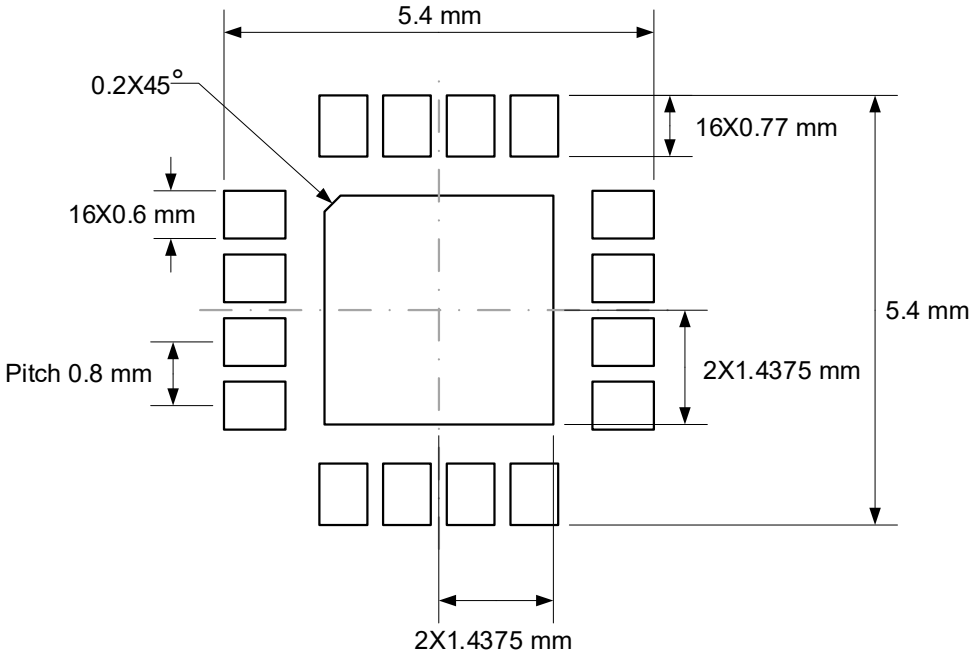






Test conditions unless otherwise noted: VBIAS = 5 V, VCC1,2,3 = 5 V, PAEN = 2 V.

PCB Mounting Pattern



GSP2P204AL PCB Layout Footprint
(Top View)

Package Dimensions

Marking: Pin 1 Indicator and SDSX Parts

Typical part markings
(Top View)

Handling Precaution

ESD countermeasure methods should be developed and used to control potential ESD damage during handling in a factory environment at each manufacturing site.

Solderability

Compatible with lead-free (260 ℃ maximum reflow temperature) soldering processes.

RoHS Compliance

This product is compliant with the EU RoHs2.0, EU Directive 2015/863.

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