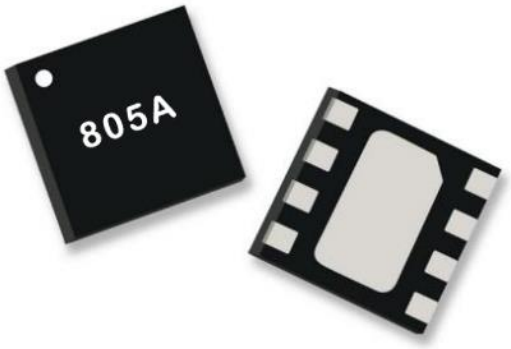
GSL805AD

0.01G-5 GHz Low Noise Amplifier



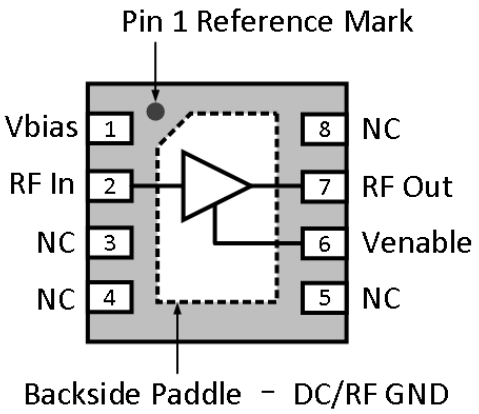
Description

The GSL805AD is a low noise amplifier (LNA) that operates in the 0.01GHz to 5GHz frequency range. The device incorporates on-chip input/output matching circuits and is fabricated with GaAs pHEMT process. Its industry-leading noise figure, together with high linearity, makes it ideal as a first stage LNA. This LNA integrates a Venable biasing capability to allow for operation in TDD applications. The GSL805AD is provided in a 2x2 mm, 8 pin DFN package.

Features

- 8 Pin 2X2 mm DFN Package
- 0.01GHz to 5GHz operation
- NF≤1.2dB across 0.01GHz to 5GHz
- >19dB gain across 0.01GHz to 4.2GHz
- >35.5dBm OIP3 @ 68mA IDD, 2.6GHz
- Shut-down mode pin with 1.8V TTL logic
- +3V to +5V supply; does not require -Vgg
- Maintains OFF state with high input power drive
- Unconditionally stable

Functional Block Diagram



Applications

- LTE / WCDMA / CDMA / GSM / Massive MIMO
- Repeaters / DAS
- TDD or FDD systems
- General Purpose Wireless

Ordering Information

- GSL805AD
- GSL805AD-TR
- GSL805AD-EVB

Recommended Operating Conditions

Parameter	Units	Min	Typ	Max
DC Supply Voltage (VDD)	V	3	5	5.5
Operational Frequency Range	GHz	0.5	——	5
Enable Voltage (Venable) On	V	0	——	0.7
Enable Voltage (Venable) Off	V	1.1	——	VDD
Operating Temperature	℃	-40	——	105

Absolute Maximum Ratings

Parameter		Units	Min	Typ	Max
DC Supply Voltage (VDD)		V	0	——	7
DC Control Voltage		V	0	——	7
RF Input Power (Pin), CW, 50ohms, T=25℃		dBm	——	——	30
RF Input Power (Pin), CW, Off State, T=25℃		dBm	——	——	30
Storage Temperature		℃	-65	——	+150
ESD Rating	HBM	V	——	1000	——
	CDM	V	——	1000	——

Electrical Specifications (VDD=5V)

Test Conditions: 50Ω system, VDD=5V, Temp=+25℃, (de-embedded data);

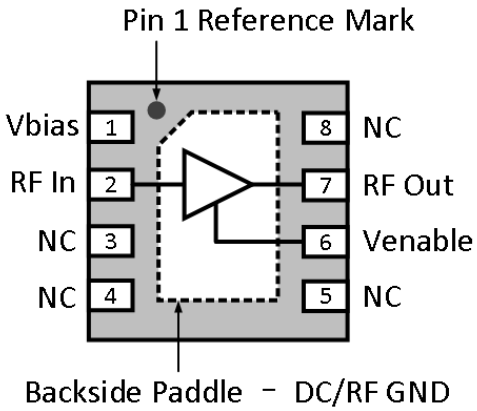
Parameter	Conditions	Units	Min	Typ	Max
Operational Frequency Range	——	GHz	0.01	——	5
Test Frequency	——	GHz	——	2.6	——
Input Return Loss	——	dB	——	11	——
Output Return Loss	——	dB	——	8.5	——
Gain	——	dB	——	22	——
Reverse ISO	——	dB	——	29	——
Off State Gain	Pin=20dBm	dB	——	-21	——
OP1dB	——	dBm	——	22	——
OIP3	Pout=+5 dBm/tone Δf=1 MHz	dBm	——	35.5	——
Noise Figure	——	dB	——	0.7	——
Drain Current	Venable=0V	mA	——	68	——
Drain Current	Venable=5V	mA	——	2	——
Venable Current	Venable=5V	uA	——	500	——
Switching Time	Switching OFF	ns	——	100	——
	Switching ON	ns	——	100	——

Electrical Specifications (VDD=3.3V)

Test Conditions: 50Ω system, VDD=3.3V, Temp=+25℃, (de-embedded data);

Parameter	Conditions	Units	Min	Typ	Max
Operational Frequency Range	——	GHz	0.01	——	5
Test Frequency	——	GHz	——	2.6	——
Input Return Loss	——	dB	——	10	——
Output Return Loss	——	dB	——	10.5	——
Gain	——	dB	——	23	——
Reverse ISO	——	dB	——	29	——
Off State Gain	Pin=20dBm	dB	——	-21	——
OP1dB	——	dBm	——	18	——
OIP3	Pout=+5 dBm/tone Δf=1 MHz	dBm	——	34	——
Noise Figure	——	dB	——	0.58	——
Drain Current	Venable=0V	mA	——	78	——
Drain Current	Venable=3.3V	mA	——	2	——
Venable Current	Venable=3.3V	uA	——	350	——
Switching Time	Switching OFF	ns	——	100	——
	Switching ON	ns	——	100	——

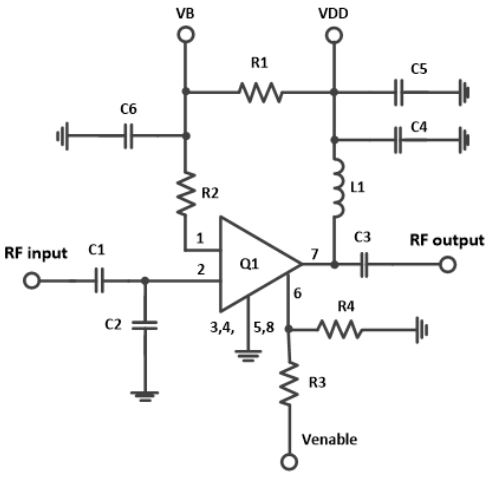
Pin Assignments and Description

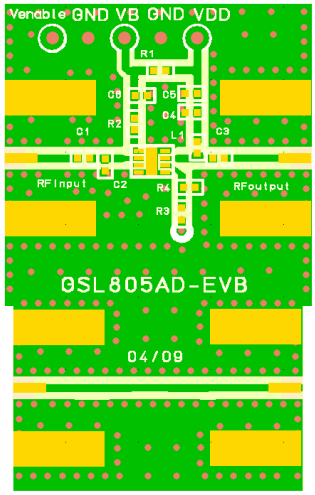


Pin	Name	Description
1	Vbias	Setting the Icq bias point for the device.
2	RF In	RF Input pin, DC Block is required.
3, 4, 5, 8	NC	No electrical connection. Provide grounded land pads for PCB mounting integrity.
6	Venable	A high voltage (≥1.1V) turning off the device.
7	RF Out	RF output pin.
Backside Paddle	DC/RF GND	Use recommended via pattern to minimize inductance and thermal resistance.

0.5G-5GHz Typical Reference Design

PCB Evaluation Board





Evaluation Board BOM

Reference Des.	Conditions	Value	Manuf.	Part Num.
PCB	N/A	N/A	SDSX	GSL805AD-EVB
Q1	N/A	N/A	SDSX	GSL805AD
R1	N/A	0Ω	Various	0402
R2	VDD=5V	2kΩ	Various	0402
	VDD=3.3V	430Ω	Various	0402
R3	N/A	0Ω	Various	0402
R4	N/A	N/A	N/A	N/A
L1	N/A	30nH	Murata	LQW15
C1	VDD=5V	330pF	Various	0402
	VDD=3.3V	30pF	Various	0402
C2	N/A	N/A	N/A	N/A
C3	N/A	330pF	Various	0402
C4	N/A	100pF	Various	0402
C5	N/A	1uF	Various	0402
C6	N/A	100nF	Various	0402

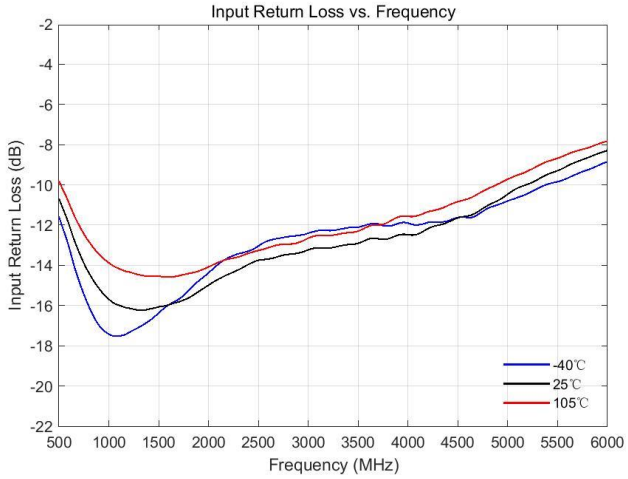
Typical Performance - VDD=5V

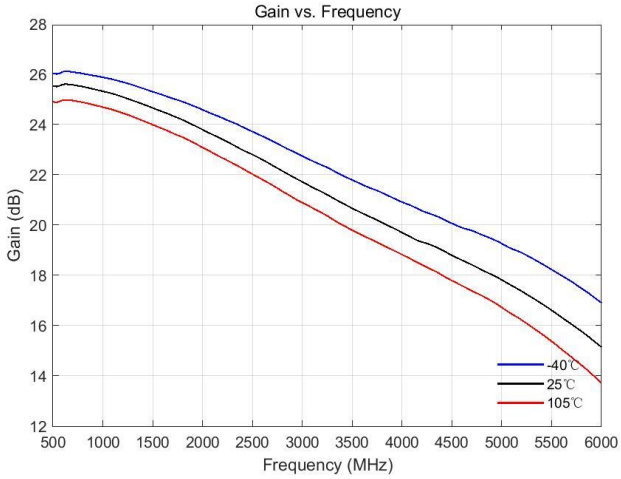
Test Conditions: 50Ω system, VDD=5V, IDD=68mA, Temp=+25℃, (de-embedded data);

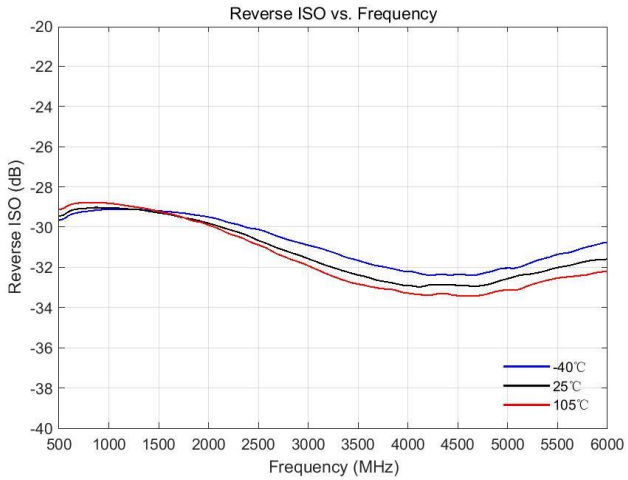
Parameter	Conditions	Units	Typical					
Frequency	——	GHz	0.6	1.9	2.6	3.5	4.2	5
Input Return Loss	——	dB	11	12	11	11.5	11	9
Output Return Loss	——	dB	9	10	8.5	9	10.5	11
Gain	——	dB	25.2	23.6	22	20.2	19	17.5
OP1dB	——	dBm	21	22	22	22	21	20
OIP3	Pout=+5 dBm/tone Δf=1 MHz	dBm	35	35	35.5	36	35	35
Noise Figure	——	dB	0.5	0.6	0.7	0.85	0.9	1.2

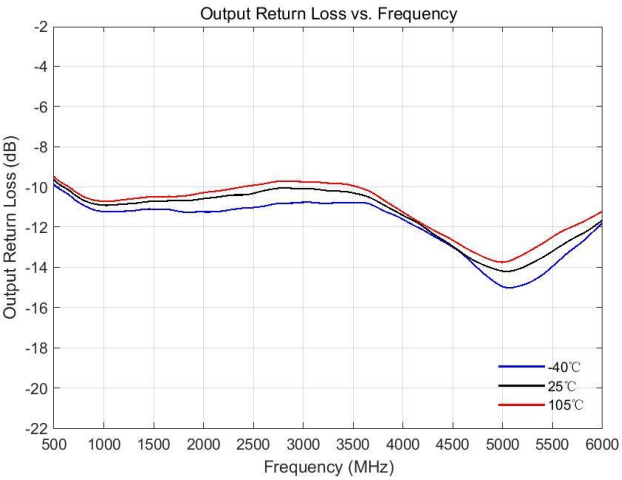
Performance Plots - VDD=5V

Test Conditions: 50Ω system, VDD=5V, IDD=68mA, (de-embedded data);



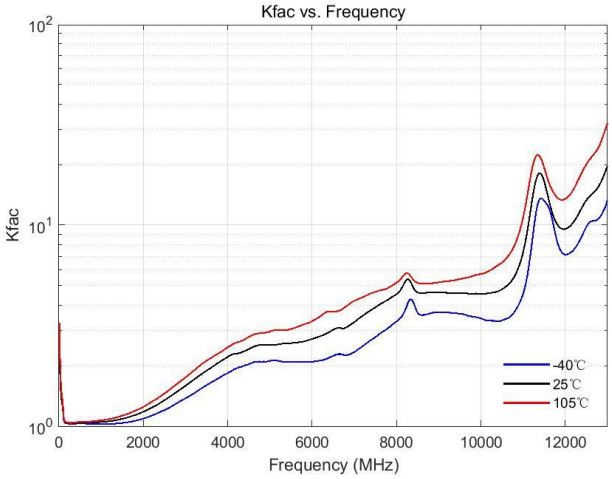


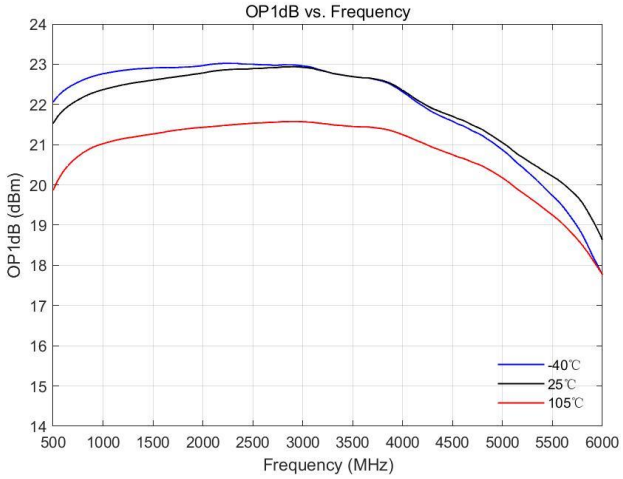


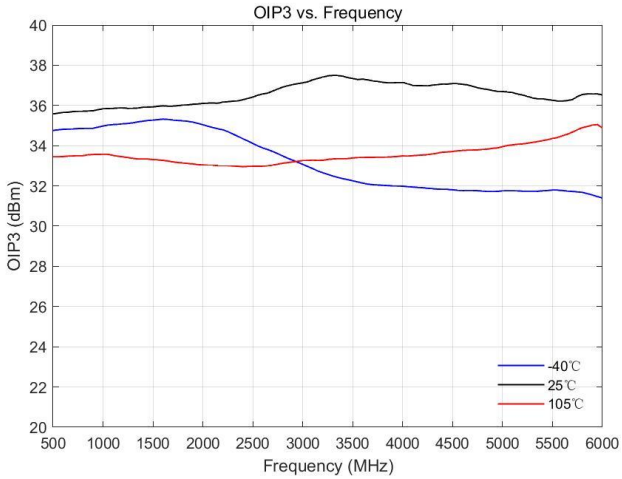


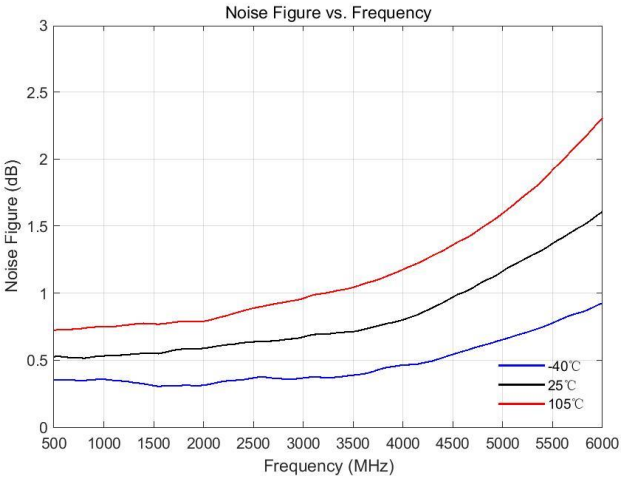
Performance Plots - VDD=5V (Cont.)

Test Conditions: 50Ω system, VDD=5V, IDD=68mA, (de-embedded data);









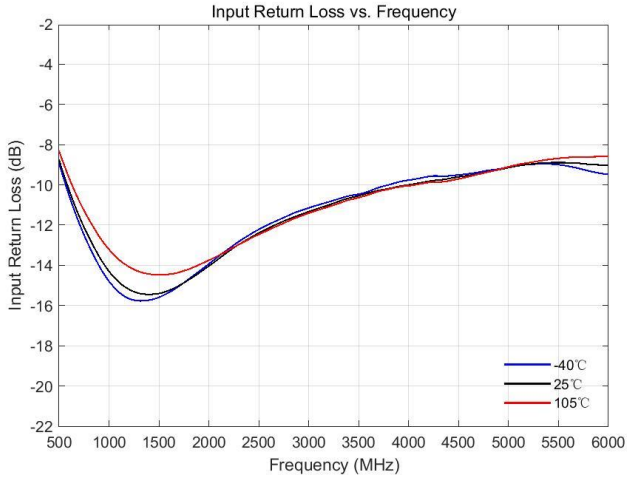
Typical Performance - VDD=3.3V

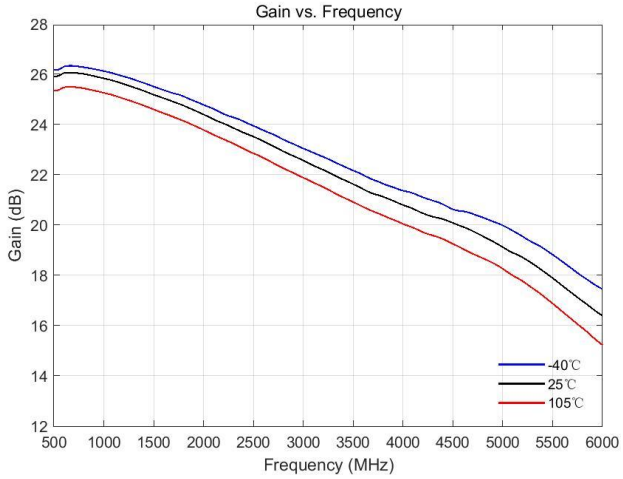
Test Conditions: 50Ω system, VDD=3.3V, IDD=78mA, Temp=+25℃, (de-embedded data);

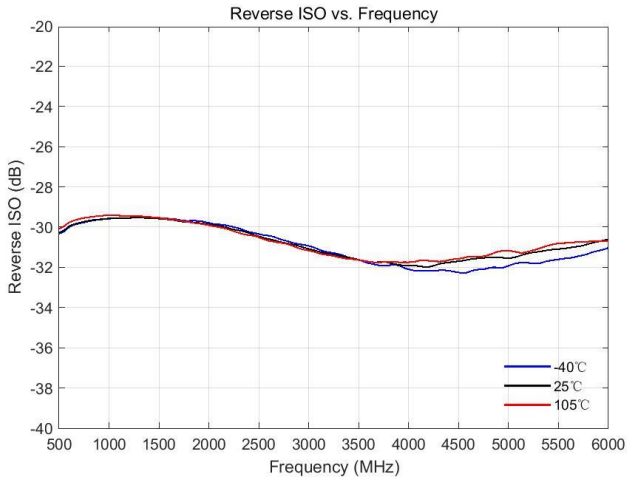
Parameter	Conditions	Units	Typical					
Frequency	——	GHz	0.6	1.9	2.6	3.5	4.2	5
Input Return Loss	——	dB	9	11	10	10	10.5	9.5
Output Return Loss	——	dB	8	10	10.5	10.5	11	12
Gain	——	dB	25.5	24	23	21	20	19
OP1dB	——	dBm	18	18	18	17.5	17.0	16
OIP3	Pout=+5 dBm/tone Δf=1 MHz	dBm	33	34.5	34	35	34	31.5
Noise Figure	——	dB	0.5	0.55	0.58	0.70	0.75	1.0

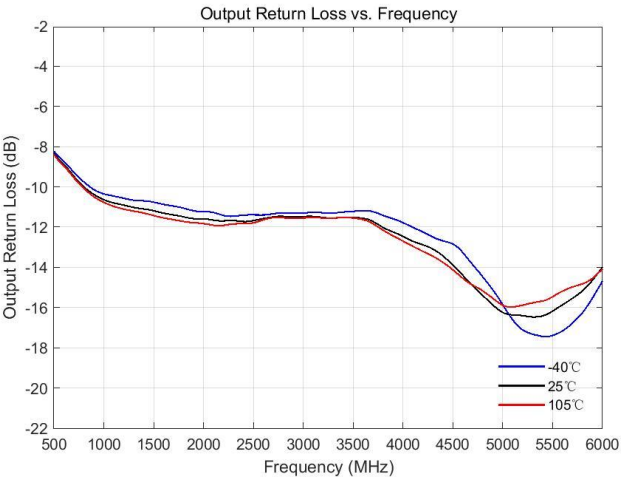
Performance Plots - VDD=3.3V

Test Conditions: 50Ω system, VDD=3.3V, IDD=78mA, (de-embedded data);



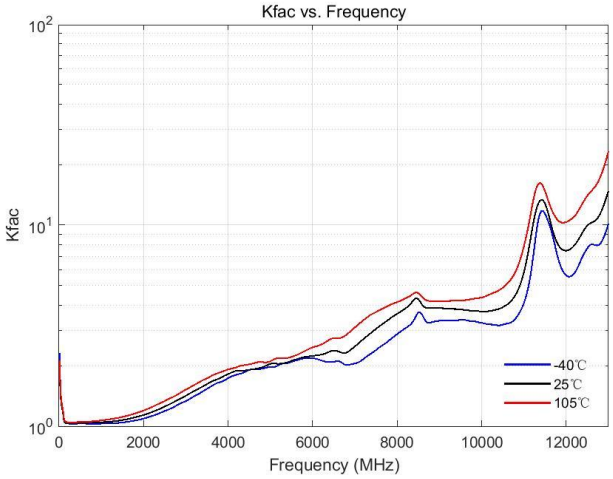


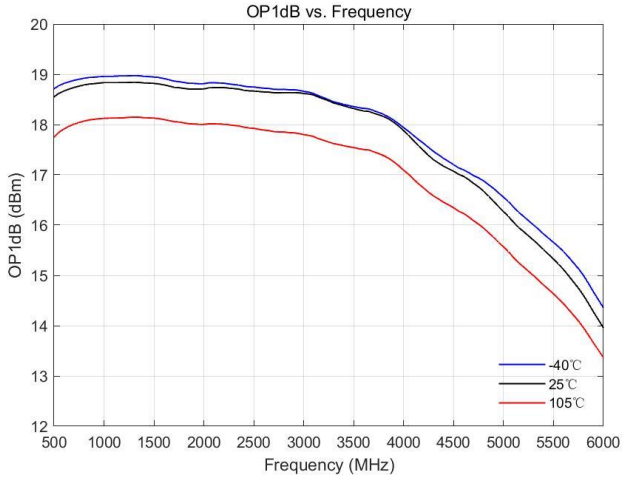


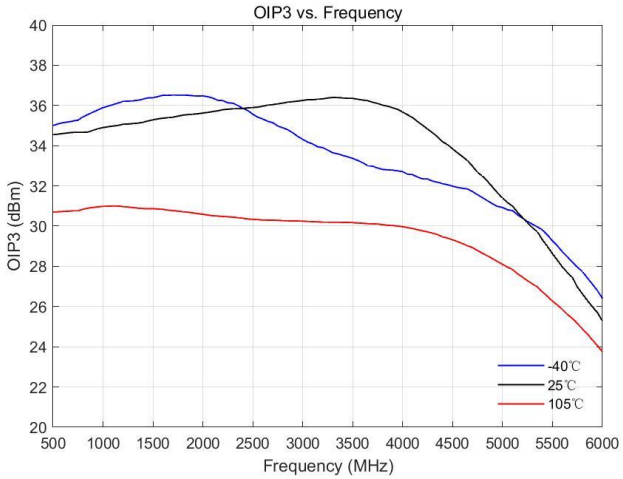


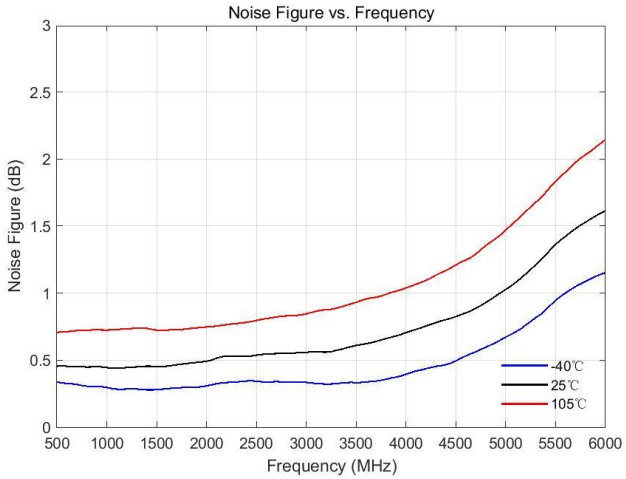
Performance Plots - VDD=3.3V (Cont.)

Test Conditions: 50Ω system, VDD=3.3V, IDD=78mA, (de-embedded data);



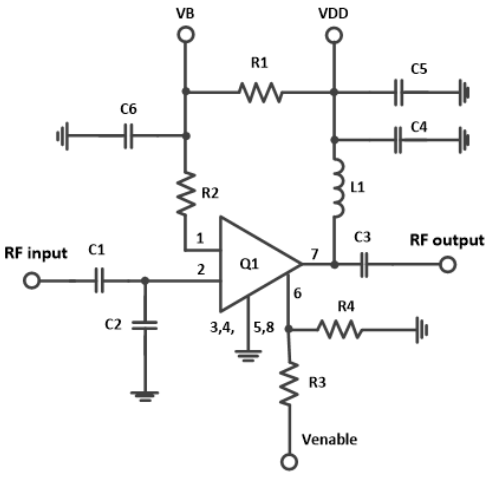


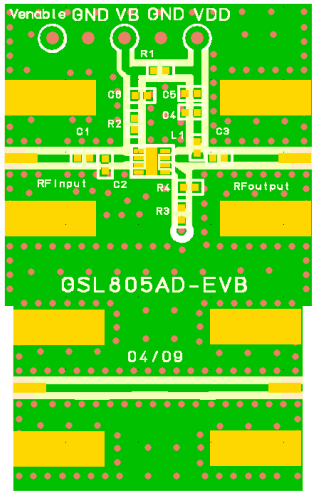




50M-2GHz Reference Design - VDD=5V

PCB Evaluation Board



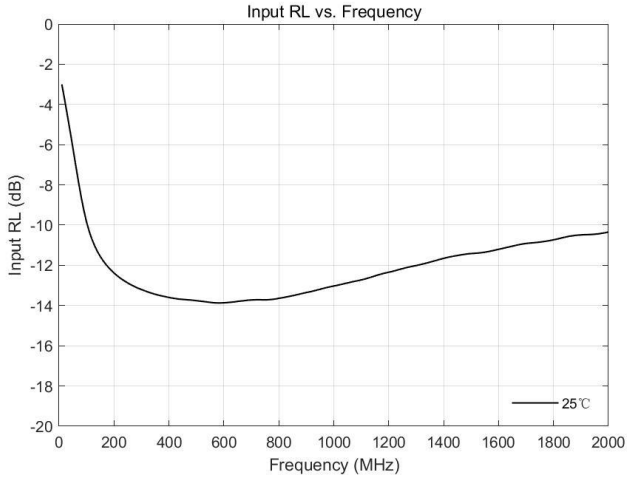


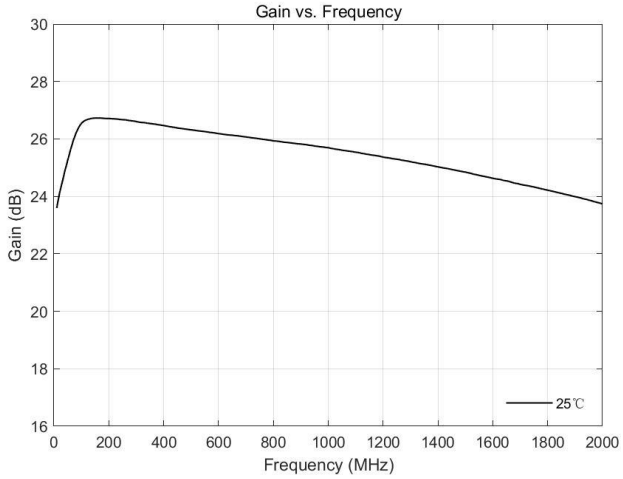
Evaluation Board BOM

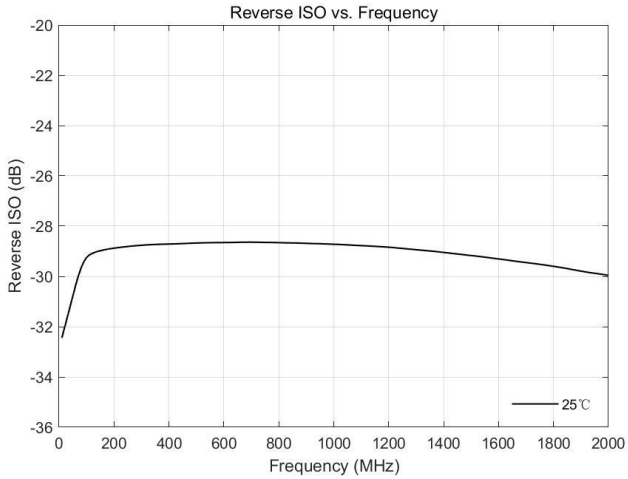
Reference Des.	Conditions	Value	Manuf.	Part Num.
PCB	50M-2G Application	N/A	SDSX	GSL805AD-EVB
Q1	50M-2G Application	N/A	SDSX	GSL805AD
R1	50M-2G Application	0Ω	Various	0402
R2	50M-2G Application	2kΩ	Various	0402
R3	50M-2G Application	0Ω	Various	0402
R4	50M-2G Application	N/A	N/A	N/A
L1	50M-2G Application	270nH	Murata	LQG 0402
C1	50M-2G Application	1uF	Various	0402
C2	50M-2G Application	N/A	N/A	N/A
C3	50M-2G Application	1uF	Various	0402
C4	50M-2G Application	100pF	Various	0402
C5	50M-2G Application	1uF	Various	0402
C6	50M-2G Application	100nF	Various	0402

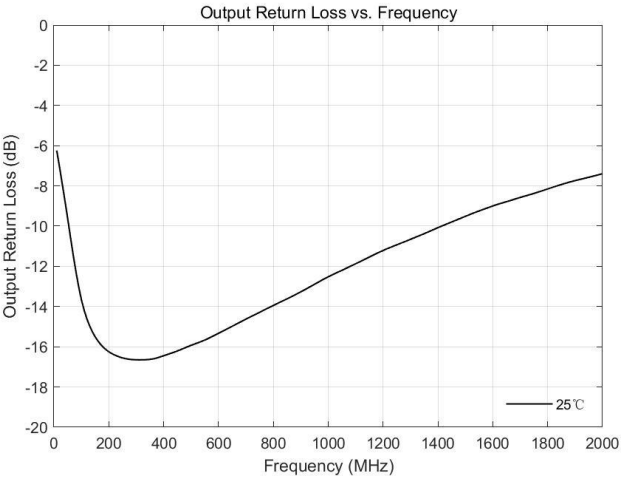
Performance Plots - VDD=5V

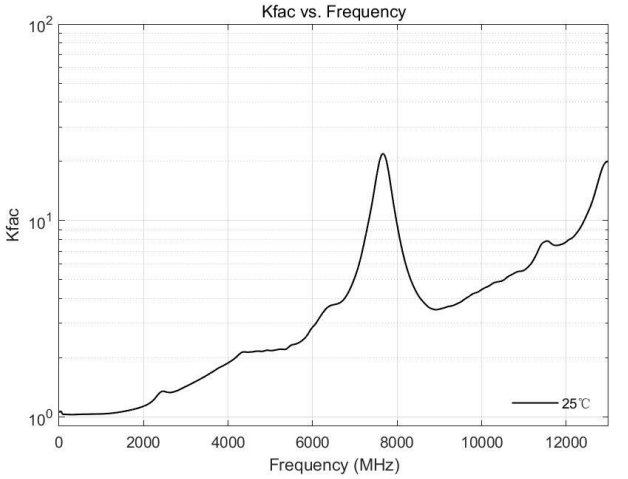
Test Conditions: 50Ω system, VDD=5V, IDD=68mA, Temp=+25℃, (de-embedded data).

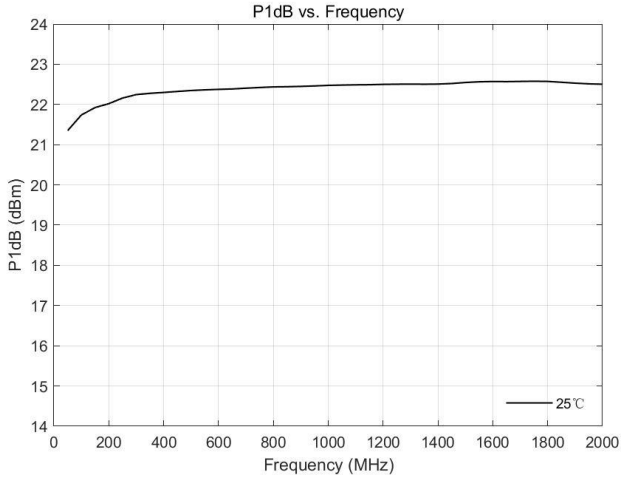






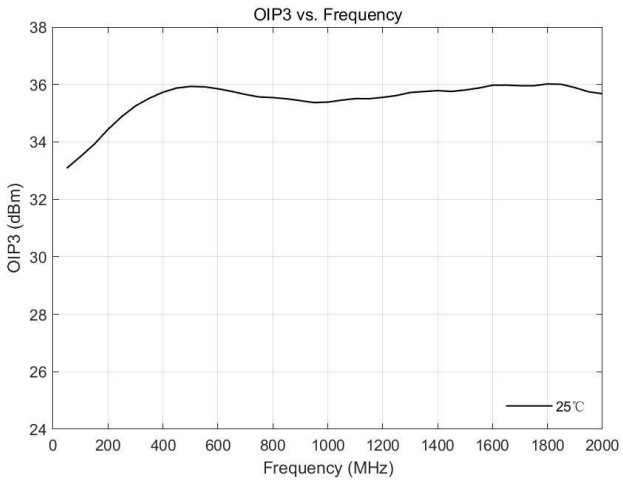


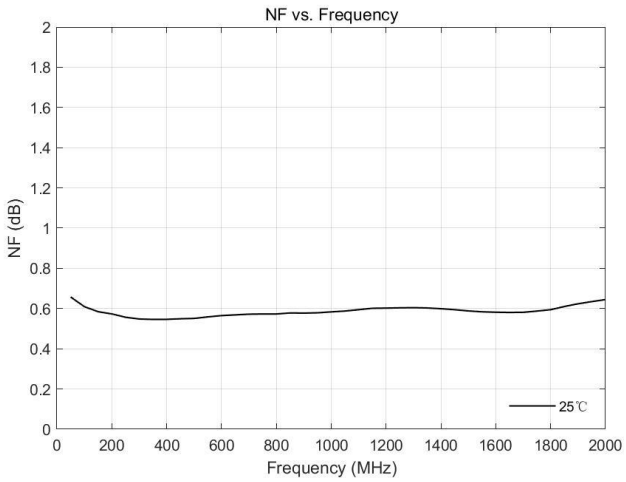




Performance Plots - VDD=5V (Cont.)

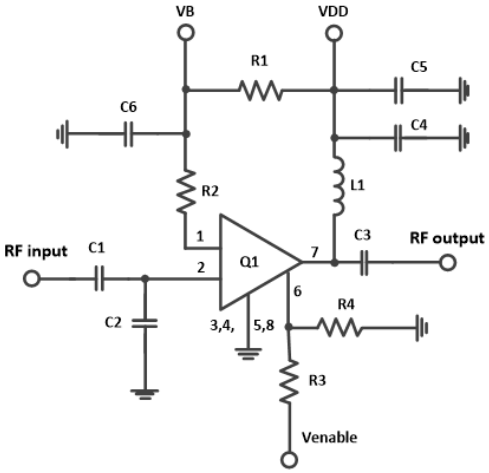
Test Conditions: 50Ω system, VDD=5V, IDD=68mA, Temp=+25℃, (de-embedded data).

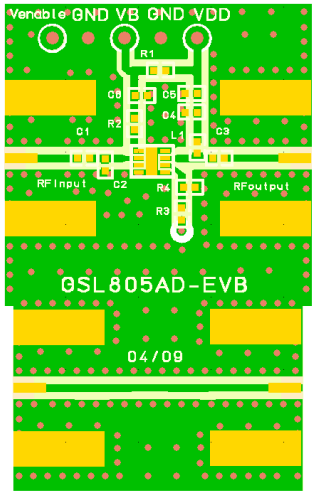




30M-700MHz Reference Design - VDD=3.3V

PCB Evaluation Board



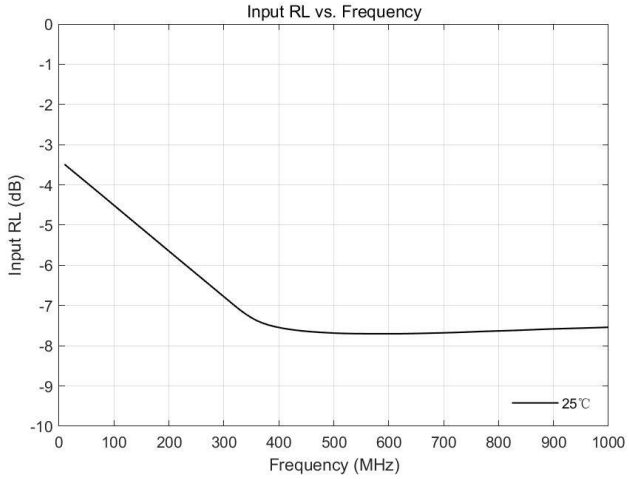


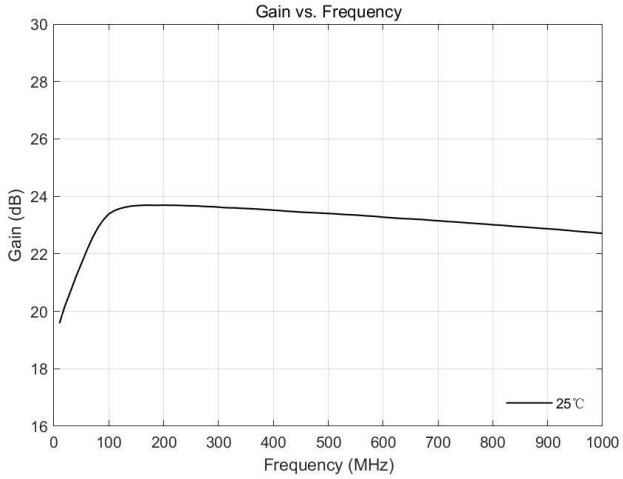
Evaluation Board BOM

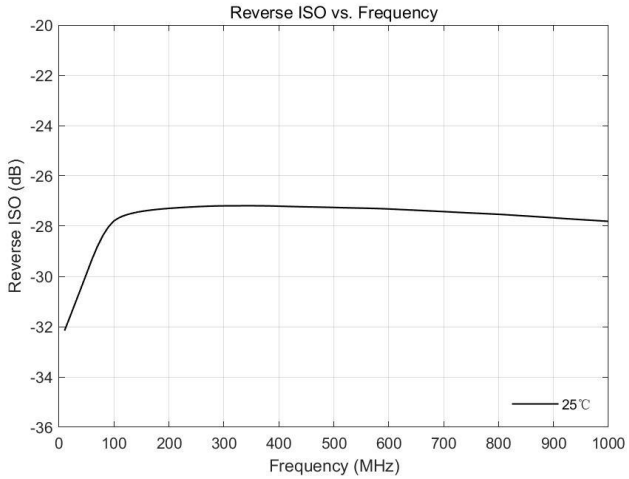
Reference Des.	Conditions	Value	Manuf.	Part Num.
PCB	30M-700M Application	N/A	SDSX	GSL805AD-EVB
Q1	30M-700M Application	N/A	SDSX	GSL805AD
R1	30M-700M Application	0Ω	Various	0402
R2	30M-700M Application	3.6kΩ	Various	0402
R3	30M-700M Application	0Ω	Various	0402
R4	30M-700M Application	N/A	N/A	N/A
L1	30M-700M Application	270nH	Murata	LQG 0402
C1	30M-700M Application	1uF	Various	0402
C2	30M-700M Application	N/A	N/A	N/A
C3	30M-700M Application	1uF	Various	0402
C4	30M-700M Application	100pF	Various	0402
C5	30M-700M Application	1uF	Various	0402
C6	30M-700M Application	100nF	Various	0402

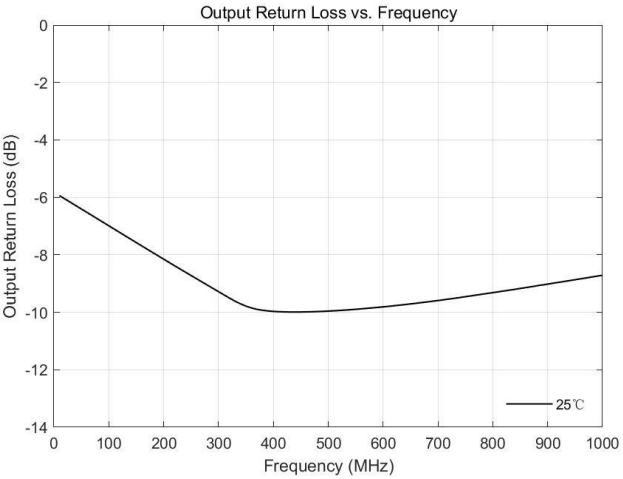
Performance Plots - VDD=3.3V

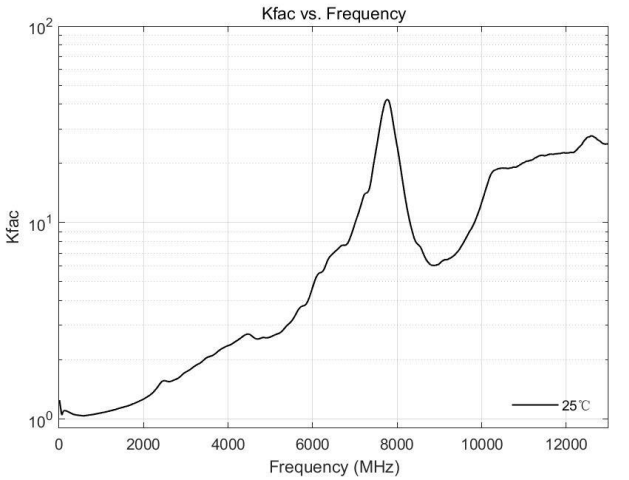
Test Conditions: 50Ω system, VDD=3.3V, IDD=19mA, Temp=+25℃, (de-embedded data).

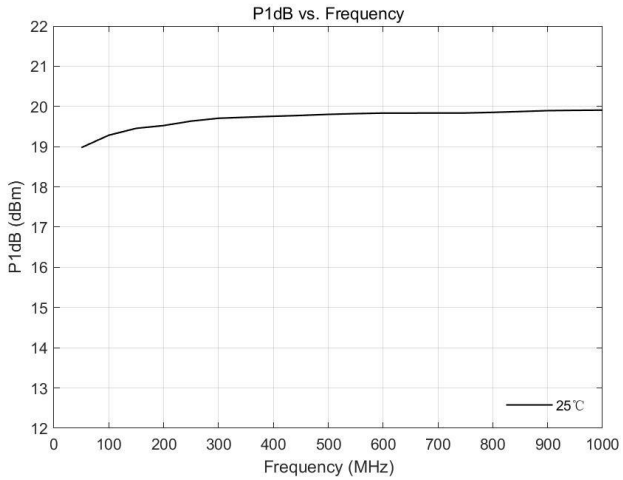






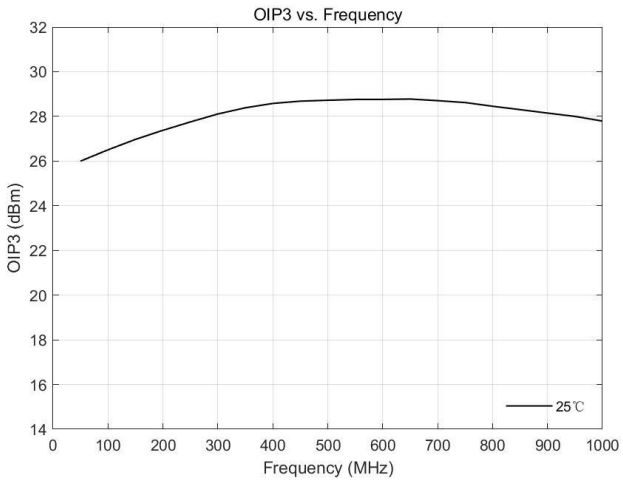


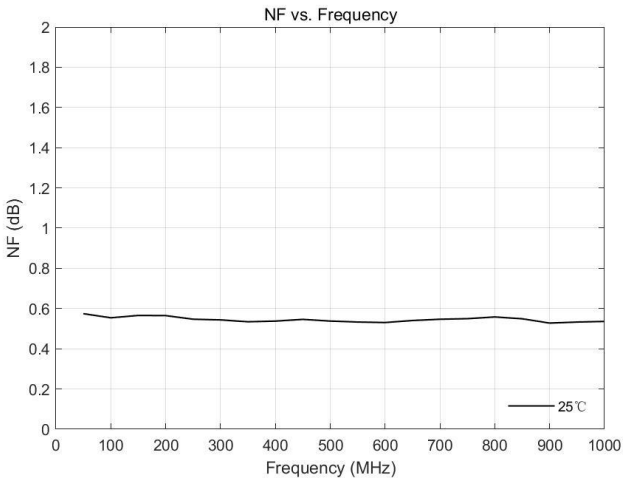




Performance Plots - VDD=3.3V (Cont.)

Test Conditions: 50Ω system, VDD=3.3V, IDD=19mA, Temp=+25℃, (de-embedded data).

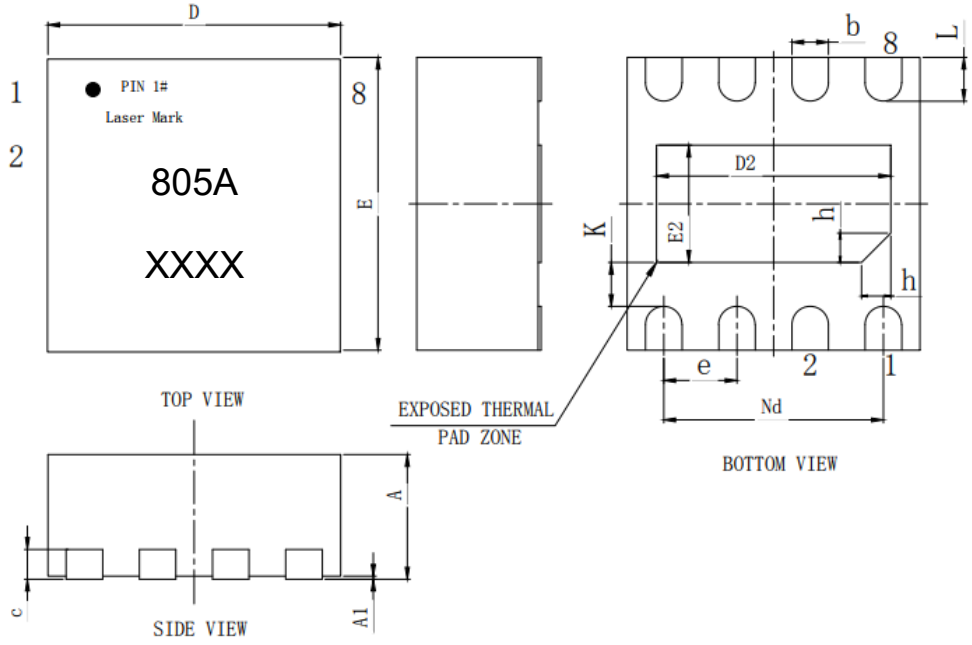




Package Marking and Dimensions

Marking: Part number – 805A

Lot code – XXXX



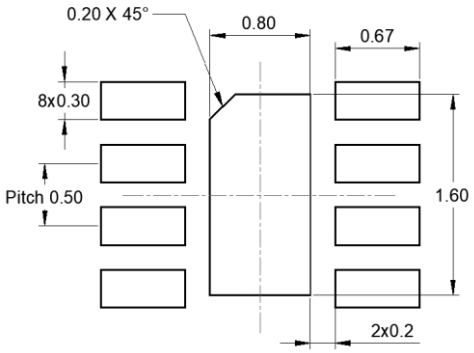
SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.80	0.85	0.90
A1	0	0.02	0.05
b	0.20	0.25	0.30
c		0.203REF	
D	1.95	2.00	2.05
D2	1.55	1.60	1.65
Nd		1.50BSC	
e		0.50BSC	
E	1.95	2.00	2.05
E2	0.75	0.80	0.85
L	0.25	0.30	0.35
K	0.25	0.30	0.35
h		0.20REF	

Notes: 1. All dimensions are in millimeters.

2. Coplanarity applies to the exposed heat sink slug as well as the terminals.

3. DFN 8 pin 2x2x0.85mm Package.

PCB Mounting Pattern



PCB Layout Footprint (Top View)

Notes: 1. All dimensions are in millimeters.

Handling Precaution

ESD countermeasure methods should be developed and used to control potential ESD damage during handling in a factory environment at each manufacturing site.

Solderability

Compatible with lead-free (260 ℃ maximum reflow temperature) soldering processes.

RoHS Compliance

This product is compliant with the EU RoHs2.0, EU Directive 2015/863.

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